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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,367	09/14/2004	Timothy H. Daubenspeck	BUR920040154US1	5366

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EXAMINER
AU, BAC H

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,367	DAUBENSPECK ET AL.	
	Examiner	Art Unit	
	Bac H. Au	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *18-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *14 September 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I invention, claims 1-17, in the reply filed on April 5, 2006 is acknowledged. The traversal is on the ground(s) that the search and the examination of the entire application can be made without serious burden. This is not found persuasive because serious burden has been appropriately established as the inventions are of separate classification and would require separate field of search. See MPEP 808.02.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The disclosure is objected to because of the following informalities: second dielectric layer “155” in para.23 line 9 should be second dielectric layer --150--; second dielectric layer “255” in para.27 line 8 should be second dielectric layer --250--; conductive liner “280” in para.32 line 4 should be conductive liner --275--; first dielectric layer “255”, second dielectric layer “245” in para.33 line 5 should be first dielectric layer --245--, second dielectric layer --250--; illustrated in “FIG. 7B” in para.48 line 5 should be illustrated in --FIG. 7C--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-8, and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roche (U.S. Pub. 2005/0048755) in view of Bohr (U.S. Pub. 2002/0064929).

Regarding claims 1 and 8, Roche [Figs.1-6] discloses a method, comprising:

(a) providing a substrate [52];

(b) forming a passivation layer [54] on a top surface of said substrate;

(c) forming an electrically conductive layer [56] on a top surface of said passivation layer;

(d) patterning said conductive layer into a plurality of wire bond pads spaced apart [Fig.3; para.17], top surfaces of said wire bond pads coplanar [It would be obvious that the bond pad surfaces are coplanar]; and

(e) forming a dielectric layer [68] on said top surface of said passivation layer in spaces between adjacent wire bond pads and on said top surfaces of said wire bond pads, said dielectric layer filling said spaces; and

(f) removing said dielectric layer from said top surface of said wire bond pads [Fig.4].

Roche failed to disclose in (f) wherein said top surface of said dielectric layer in said spaces coplanar with said top surfaces of said wire bond pads. However, Bohr [Figs.2c-d] discloses removing said dielectric layer [212] from said top surface of said wire bond pads, said top surface of said dielectric layer in said spaces coplanar with said top surfaces of said wire bond pads.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Bohr into the method of Roche to include in removing said dielectric layer from said top surface of said wire bond pads and making said top surface of said dielectric layer in said spaces coplanar with said top surfaces of said wire bond pads. The ordinary artisan would have been motivated to modify Roche in the manner set forth above for at least the purpose of providing a planar surface to facilitate the deposit of subsequent layers that are difficult to deposit into high aspect ratio gaps with a desired thickness [Bohr; para.6].

Regarding claims 3-7, and 10-16, Roche and Bohr disclose

recessing said wire bond pads below said top surfaces of said dielectric layer in said spaces [Roche; fig.6];

forming a final dielectric layer [72] on said substrate, said dielectric layer and said wire bond pads [Roche; fig.5]; and

forming openings [74] in said final dielectric layer to expose less than an entire portion of each said wire bond pad in said openings [Roche; fig.5];

wherein said final dielectric layer comprises a material selected from the group consisting of polyimide and photo-sensitive polyimide [Roche; para.22];

wherein said dielectric layer [68] comprises a layer of silicon oxide, a layer of silicon nitride or combinations thereof [Roche; para.20];

wherein said wire bond pads comprise aluminum, aluminum copper alloy, copper, gold, tantalum, tantalum nitride or combinations thereof [Roche; paras.3,16].

4. Claims 2, 9, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roche (U.S. Pub. 2005/0048755) and Bohr (U.S. Pub. 2002/0064929) as applied to claims 1 and 8 above, and further in view of Peters (U.S. Pat. 6521530).

Regarding claims 2, 9, and 17, Roche and Bohr disclose electrical interconnects and aspects of integrated circuit manufacturing as discussed above, but fail to explicitly disclose wherein the method

further including: recessing said dielectric layer in said spaces below said top surfaces of said wire bond pads;

further including between steps (b) and (c), forming via openings in said passivation layer exposing regions of electrically conductive wires in said substrate;

wherein step (d) fills said via openings with said electrically conductive layer; and

wherein step (d) includes forming each wire bond pad over at least one said via opening.

However, Peters [Figs.7a-e] discloses the method

further including: recessing said dielectric layer in said spaces below said top surfaces of said wire bond pads [Fig.7e];

further including between steps (b) and (c), forming via openings [708] in said passivation layer [706] exposing regions of electrically conductive wires [704] in said substrate;

wherein step (d) fills said via openings with said electrically conductive layer [710]; and

wherein step (d) includes forming each wire bond pad over at least one said via opening [Fig.7e].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Peters into the method of Roche and Bohr wherein further including: recessing said dielectric layer in said spaces below said top surfaces of said wire bond pads; further including between steps (b) and (c), forming via openings in said passivation layer exposing regions of electrically conductive wires in said substrate; wherein step (d) fills said via openings with said electrically conductive layer; and wherein step (d) includes forming each wire bond pad over at least one said via opening. The ordinary artisan would have been motivated to modify Roche and Bohr in the manner set forth above since forming interconnects with conductive vias and raised bond pads are well-known in integrated circuit manufacturing.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BHA

Zandra V. Smith
Supervisory Patent Examiner
21 April 2006